Docket No.: 50006-188 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Hans Jurgen MATTAUSCH, et al.	:	Confirmation Number:
Serial No.:	:	Group Art Unit:
Filed: February 27, 2004	:	Examiner:

For: MEMORY WITH SYNCHRONOUS BANK ARCHITECTURE

INFORMATION DISCLOSURE STATEMENT

Mail Stop Information Disclosure
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

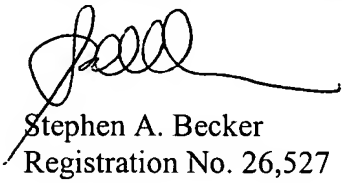
The relevance of each reference, if any, is discussed in the present specification.

Serial No.:

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
50006-188	
APPLICANT: **Hans Jurgen MATTAUSCH, et al.**	
FILING DATE: **February 27, 2004**	GROUP

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US			
		US			
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes3 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		H.J. MATTAUSCH, "Hierarchical architecture for area-efficient integrated *N*-port memories with latency-free multi-gigabit per second access bandwidth", Electronics Letters, 19th August 1999, Vol. 35, No. 17, pages 1-2.	
		N. OMORI et al., "Compact central arbiters for memories with multiple read/write ports", Electronics Letters, 21st June 2001, Vol. 37, No. 13, pages 811-813 (w/ English Translation).	
		H.J. MATTAUSCH, "Area-Efficient Multi-Port SRAMs for On-Chip Data-Storage with High Random-Access Bandwidth and Large Storage Capacity", IEICE Trans. Electron., Vol. E84-C, No. 3, March 2001, pages 410-418.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.